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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,717	10/31/2003	Krzysztof Nauka	200310817-1	1558

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EXAMINER	
PHAM, VAN T	

ART UNIT	PAPER NUMBER
2627	

DATE MAILED: 11/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,717	NAUKA ET AL.	
	Examiner	Art Unit	
	VAN T. PHAM	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/06/2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7,9-12,25,26,28 and 29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,9-12,25,26,28 and 29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Appeal Brief and Arguments

1. In response to the Appeal Brief and arguments, see Appeal Brief, filed 09/06/2006, with respect to the rejection(s) of:

Claims 9, 11-12, 28-29 have been consider but they are not persuasive.

Claim 9: "The office action cites a first passages at col. 3, lines 52-58 and a second passage at col. 10, lines 53-61 of Kasanuki. The first passage discloses a circuit 7 for performing erasure, but does not teach or suggest that the circuit can perform block and bulk erasures. The relevance of the second passage is not clear, as it only discusses the choice of material for the probe, and the necessity of a sharp probe tip. Because Kasanuki does not teach or suggest all of the claim features of claim 9, claim 9 should be allowed over Kasanuki" (see page 7). Applicant's definition of block erasure in paragraph [0030] is "a block erasure can be performed be dragging the probe tip along the ferroelectric layer across multiple bits" and Kasanuki discloses

> "In an information processing apparatus using a recording medium based on the principles of an STM and formed from a ferroelectric substance, information is written by applying an electric field based on the principles of an STM. Reading of information is performed by a complicated method in which a recording layer is heated by laser beam irradiation or high-frequency heating, the recording medium is activated pyroelectrically, and signals which occur are detected by an ultra-high resolution electrometer probe in a standard electrometer. It cannot be said that this is a simple method. The information processing apparatus shown in FIG. 13 has a problem in that when a probe or a recording medium is scanned two-dimensionally in X and Y directions, resonance is likely to occur in the scanning mechanism if the scanning frequency increases.

Claims 11 and 28: Applicant's asserted, "Paragraph 58 discloses that the dielectric film 12 may be made of a ferroelectric material, and paragraph 72 discloses that the electrode 13 may be formed on a silicon substrate. The dielectric thin film 12 is on one side of the electrode 13,

and the silicon substrate is on the other side of the electrode. Therefore, the silicon substrate and the thin dielectric film 12 do not form an electrical junction". This is not convincing because the silicon substrate and the thin film 12 do form an electrical junction. There is a potential difference to ground at the substrate that is sensed and hence this is the electrical junction (see Cho Fig. 1).

Claims 12 and 29: Applicant's asserted, "Data can be reproduced by demodulating the oscillator signal and synchronizing the demodulated signal with ac signals that are generated by ac generators 15a-15n. Although Cho discloses that the ac signals are applied to the probes 14a-14n, Cho does not teach or suggest detecting changes in a non-linear component of a dielectric constant". Sensed using AC, capacitance/inductors must be non-linear (see Cho paragraph [0071] and [0075]).

However, Applicant's request for reconsideration of the finality of the rejection of the last Office action of claims 7, 10, 25-26 is persuasive and, therefore, the finality of that action is withdrawn and a new ground of rejection is made on claims **7, 10, and 25-26**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Kasanuki et al. (US 5,481,527).

Regarding claim 9, Kasanuki discloses a data storage device comprising a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1 and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col. 8, line 21); and a circuit for causing the conductive probe to perform block and bulk erasure (see response above).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being anticipated by Kasanuki et al. (US 5,481,527) in view of Imaneka et al. (US 6,945,633).

Regarding claim 7, Kasanuki discloses a data storage device comprising: a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1

and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col.8, line 21).

Imanaka Fig. 8B, discloses a data storage device comprising: a protective layer (see layer 33) covering the ferroelectric layer (see layer 22).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a protective layer (see layer 33) covering the ferroelectric layer (see layer 22) in Kasanuki as suggested by Imanaka, the motivation being in order for preventing reduction environment (see Kasanuki col. 5, lines 40-55).

6. Claims 11-12, 28-29 are rejected under 35 U.S.C. 103(a) as being anticipated by Cho (US 2003/0053400) in view of Kasanuki et al. (US 5,481,527).

Regarding claim 11 and 28, see Fig. 2, Cho discloses a data storage device comprising: a conductive probe having a tip (see Fig. 2, probe 14, and col. 1, [0012]); a substrate (see Fig. 2, element 12) including a semiconductor portion; and a data storage medium including a layer of poled ferroelectric material for storing data, the ferroelectric layer on the substrate, between the tip and the substrate (see Fig. 2, elements 11-13 and col. 4, [0049]), a read circuit for using the probe to sense changes in capacitance or leakage current of the junction (see Figs. 1-5, and elements Csa, Csb,...,Csn and [0071-[0075]).

Kasanuki disclose a data storage device comprising: a substrate including a semiconductor portion (see Fig. 1, element 4, col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), and the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57-col.8, line 21, and see response for claim 7).

Regarding claims 12 and 29, see rejection above of claims 11 and 28 and a read circuit for using the probe to apply an ac signal to local areas on the ferroelectric material, and detect changes in a non-linear component (see response above).

7. Claims 10, 25-26 are rejected under 35 U.S.C. 103(a) as being anticipated by Kasanuki et al. (US 5,481,527) in view of Hamann et al. (US 6,597,639).

Regarding claim 10, Kasanuki discloses a data storage device comprising: a conductive probe having a tip (see Fig. 1, elements 1-2); a substrate including a semiconductor portion (see Fig. 1, element 4 and col. 7, lines 23-28); and a data storage medium including a layer of poled ferroelectric material for storing data (see Fig. 1, element 3), the ferroelectric layer on the substrate (see Fig. 1, element 3-4), between the tip and the substrate (see Fig. 1, elements tip 1 and substrate 4), the semiconductor portion and the ferroelectric layer forming an electrical junction (see col. 7, lines 23-28, col. 7, line 57- col.8, line 21); and a circuit for causing the conductive probe to perform block and bulk erasure operations (see col. 3, line 50-58, noted that in the specification define a block erasure is "a block erasure can be performed by dragging the probe tip along the ferroelectric layer across multiple bits (see [0030]).

Hamann discloses a means for heating the ferroelectric material above its Curie temperature (see col. 2, lines 1-23).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a means for heating the ferroelectric material above its Curie temperature in Kasanuki as suggested by Hamann, the motivation being in order to lower the ferroelectric coerctivity of the ferroelectric media (see Hamann col. 2, lines 10-13).

Regarding claim 25, the combination of Kasanuki and Hamann, discloses a method of

writing information to a layer of poled ferroelectric material, the method comprising using a probe to create local polarization changes in the material, the probe having a tip diameter no more than several nanometers (see Kasanuki Figs. 1-5 and col. 5, [0004], [0019], [0062] and [0065], [0070] note that by using the tip to write information on the particles which particles size is around 10 nanometers; therefore the tip size is no more than several nanometers); and heating the ferroelectric layer above its Curie temperature, whereby block erasure of the ferroelectric layer is performed (see rejection above of claim 10).

Regarding claims 26, see rejection above of claims 10 and 25.

Cited References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The cited references relate to information processing apparatus with ferroelectric rewritable recording medium and methods for conducting between a scanned-probe and storage medium.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN T. PHAM whose telephone number is 571-272-7590. The examiner can normally be reached on Monday-Friday from 9:00-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VP

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER